

TITLE: 1.25G SFP ZX 1550nm 80km Transceiver	DOC No. RFD-20250417014-002	
	REVISION : 01	AUTHORIZED BY : Albert Lin
	DATE : 2025.04.17	CLASSIFICATION : Optical Transceiver

1. DESCRIPTION

1G ZX is a high performance, cost effective module, which is transmission distance up to 80km on SMF. The transceiver consists of two sections: The transmitter section incorporates a 1550nm DFB driver. The receiver section consists of a PIN photodiode integrated with a transimpedance preamplifier (TIA). The module is hot pluggable into the 20-pin connector. The high-speed electrical interface is based on low voltage logic, with nominal 100 Ohms differential impedance and AC coupled in the module. The optical output can be disabled by LVTTTL logic high-level input of TX_DIS. Loss of signal (RX_LOS) output is provided to indicate the loss of an input optical signal of receiver.

2. PRODUCT FEATURES

- Compliant with SFF-8074i and SFF-8472
- Compliant with SFP MSA specification
- Digital Diagnostic Monitoring available
- Uncooled 1550nm DFB Laser
- Up to 1.25Gb/s data links
- Up to 80km on 9/125μm SMF
- Duplex LC connector compliant
- Single +3.3V DC power supply
- Hot-pluggable SFP footprint
- Class 1 laser safety certified
- Low power dissipation
- Operating temperature Options: 0 ~ +70°C

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3. PRODUCT DESCRIPTION

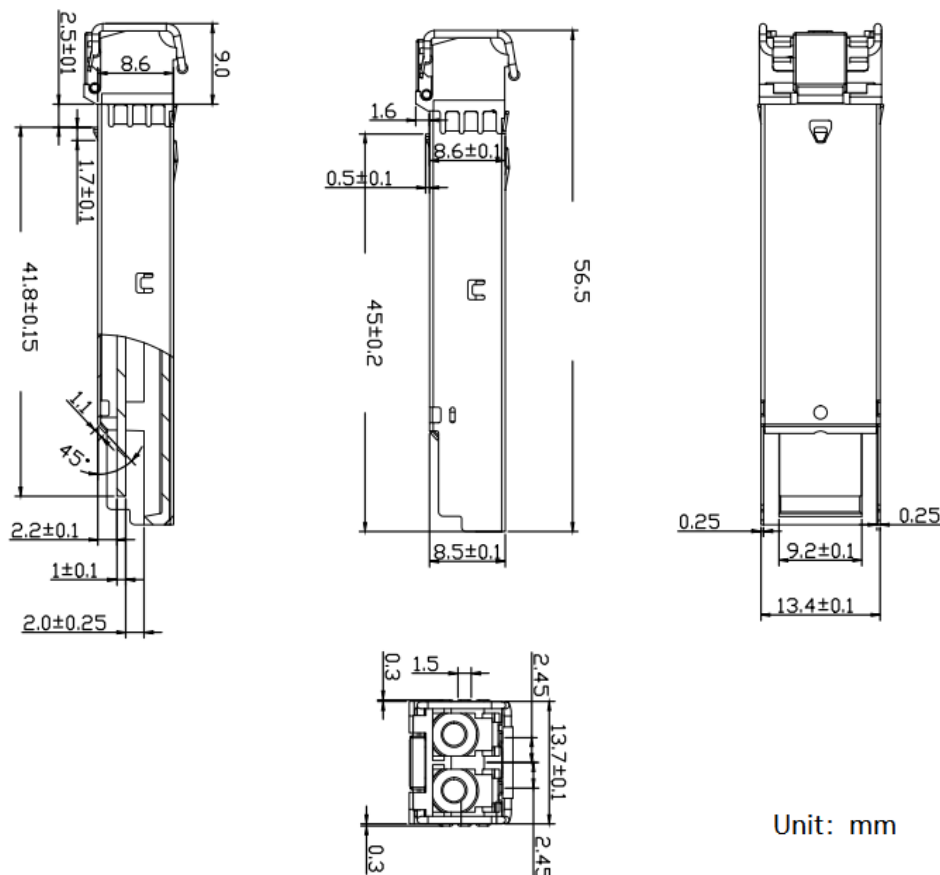
3.1 PRODUCT NAME AND SERIES NUMBER(S)

1G SFP ZX 80km Transceiver

JPC P/N	Wavelength(nm)	Distance	Media	Power (dBm)	Sen. (dBm)	Connector	Tem.
P58**0ARCV80-1	1550nm	80Km	SMF	0 ~ 5	-25	LC	C

Note-1 : ** Indicates the customer code.

3.2 DIMENSIONS, MATERIALS, PLATINGS AND MARKING



Unit: mm

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4. APPLICABLE DOCUMENTS AND SPECIFICATIONS

- 1000BASE Ethernet
- Switch to Switch Interface
- Other Optical Links

5. Absolute Maximum Ratings & Recommended Operating Conditions

Absolute Maximum Ratings				
Parameter	Symbol	Min.	Max.	Unit
Storage Temperature	T _S	-40	85	°C
Storage Ambient Humidity	H _A	5	95	%
Power Supply Voltage	V _{CC}	-0.5	4	V
Signal Input Voltage	-	-0.3	V _{CC} +0.3	V

Recommended Operating Conditions					
Parameter	Symbol	Min.	Typical	Max.	Unit
Operating Case Temperature(C-temp)	TC	0	-	70	°C
Power Supply Voltage	V _{CC}	3.14	3.3	3.46	V
Power Supply Current	I _{CC}	-	-	330	mA
Power Dissipation	P	-	-	1.1	W
Data Rate	-	-	1.25		GBd
Transmission Distance	-	-	-	80	km
Coupled Fiber	Single Mode Fiber				9/125um

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Transmitter Operating Characteristic-Optical, Electrical

Parameter		Symbol	Min.	Typical	Max.	Unit	Note
Center Wavelength		λ_c	1530	1550	1570	nm	
Laser Off Power		P _{off}	-	-	-30	dBm	
Average Optical Power		P _{avg}	+0	-	+5	dBm	
Spectral Width (-20dB)		-	-	-	1	nm	
Extinction Ratio		ER	9	-	-	dB	
Tx Input Diff Swing		V _I	300	—	2200	mV	
Tx_Disable	Disable	-	2	-	VCC	V	
	Enable	-	VEE	-	VEE+0.8	V	

Receiver Operating Characteristic-Optical, Electrical

Parameter		Symbol	Min.	Typ.	Max.	Unit	Note
Center Wavelength		λ_r	1260		1600	nm	
Receiver Sensitivity (OMA)		S	-	-	-25	dBm	
LOS Assert		LOS A	-35	-	-	dBm	
LOS Dessert		LOS D	-	-	-26	dBm	
LOS Hysteresis		LOSH	0.5	-	6	dB	
Overload		P _{ov}	-3	-	-	dBm	
Return Loss of Receiver		-	12	-	-	dB	
Rx Output Diff Swing		V _o	500	-	1200	mV	

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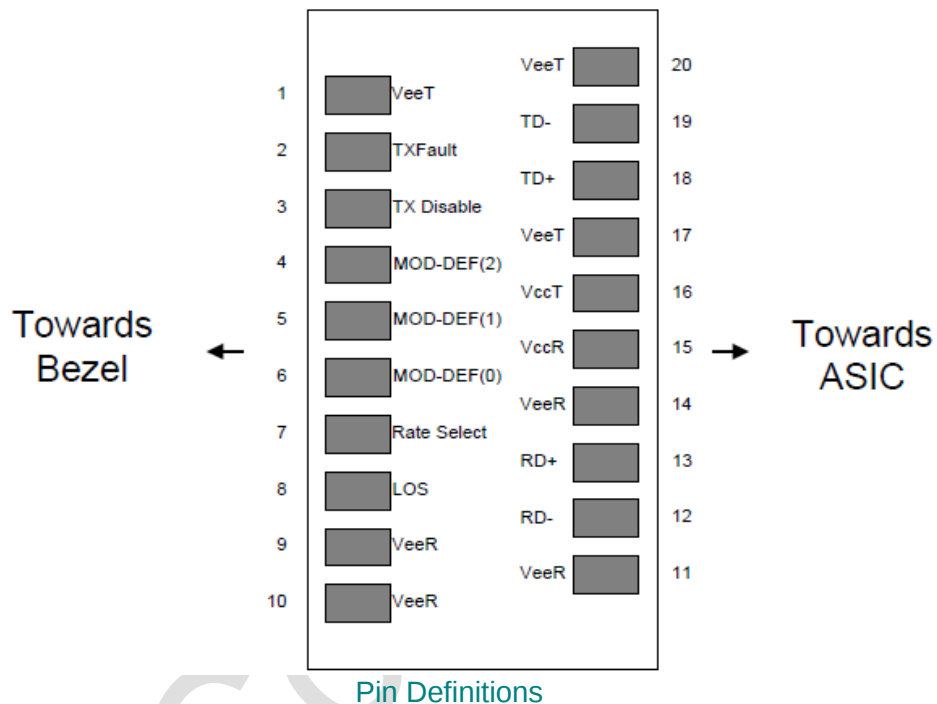
Control and Status I/O Timing Characteristics					
Parameter	Symbol	Min.	Typ.	Max.	Note
TX Disable Assert Time	t_off	-	100	μs	Note1
TX Disable Negate Time	t_on	-	2	ms	Note2
Time to initialize including reset of TX_Fault	t_init	-	300	ms	Note3
TX Fault Assert Time	t_fault	-	1	ms	Note4
Tx_Fault Reset	t_reset	10	-	μs	Note5
LOS Assert Time	t_loss_on	-	100	μs	Note6
LOS Deassert Time	t_loss_off	-	100	μs	Note7
Serial ID Clock Rate	f_serial_clock	100	400	kHz	Note8

Notes:

1. Time from rising edge of TX Disable to when the optical output falls below 10% of nominal
2. Time from falling edge of TX Disable to when the modulated optical output rises above 90% of nominal
3. From power on or negation of TX Fault using TX Disable
4. Time from fault to TX fault on
5. Time TX Disable must be held high to reset TX_fault
6. Time from LOS state to RX LOS assert
7. Time from non-LOS state to RX LOS deassert.
8. Time from rising or falling edge of Rate Select input until receiver bandwidth is in conformance with appropriate specification

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6. Applications Note:



Pin Assignment

Pin	Name	Description	Notes
1	VeeT	Module Transmitter Ground	Note1
2	TX_Fault	Module Transmitter Fault	Note2
3	TX_Disable	Transmitter Disable; Turns off transmitter laser output	Note3
4	SDA	2-wire Serial Interface Data Line (Same as MOD-DEF2 as defined in the INF-8074i)	Note4
5	SCL	2-wire Serial Interface Clock (Same as MOD-DEF1 as defined in the INF-8074i)	Note4

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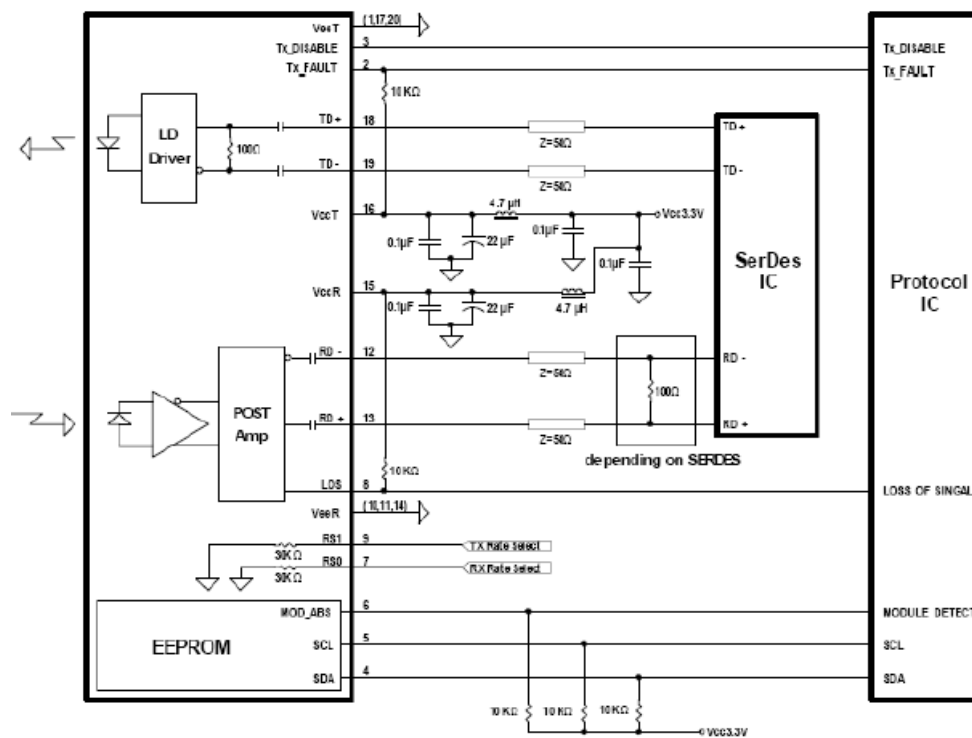
6	MOD_ABS	Module Absent, connected to VeeT or VeeR in the module	Note5
7	RS	Rate Select, optionally controls SFP module receiver. When High input data rate 10.3GBd and when LOW input data rate 1.25GBd.	Note6
8	RX_LOS	Receiver Loss of Signal Indication (In FC designated as RX_LOS, in SONET designated as LOS, and in Ethernet designated at Signal Detect)	Note2
9	VeeR	Module Receiver Ground	Note1
10	VeeR	Module Receiver Ground	Note1
11	VeeR	Module Receiver Ground	Note1
12	RD-	Receiver Inverted Data Output	
13	RD+	Receiver Non-Inverted Data Output	
14	VeeR	Module Receiver Ground	Note1
15	VccR	Module Receiver 3.3 V Supply	
16	VccT	Module Transmitter 3.3 V Supply	
17	VeeT	Module Transmitter Ground	Note1
18	TD+	Transmitter Non-Inverted Data Input	
19	TD-	Transmitter Inverted Data Input	
20	VeeT	Module Transmitter Ground	Note1

Notes:

1. The module signal ground pins, VeeR and VeeT, shall be isolated from the module case.
2. This pin is an open collector/drain output pin and shall be pulled up with 4.7k-10kohms to Host_Vcc on the host board. Pull ups can be connected to multiple power supplies, however the host board design shall ensure that no module pin has voltage exceeding module VccT/R + 0.5 V.
3. This pin is an open collector/drain input pin and shall be pulled up with 4.7k-10kohms to VccT in the module.
4. See sff-8472 4.2 2-wire Electrical Specifications.
5. This pin shall be pulled up with 4.7k-10kohms to Host_Vcc on the host board.
6. If implementing SFF-8079 pin 7 are used for RS0.

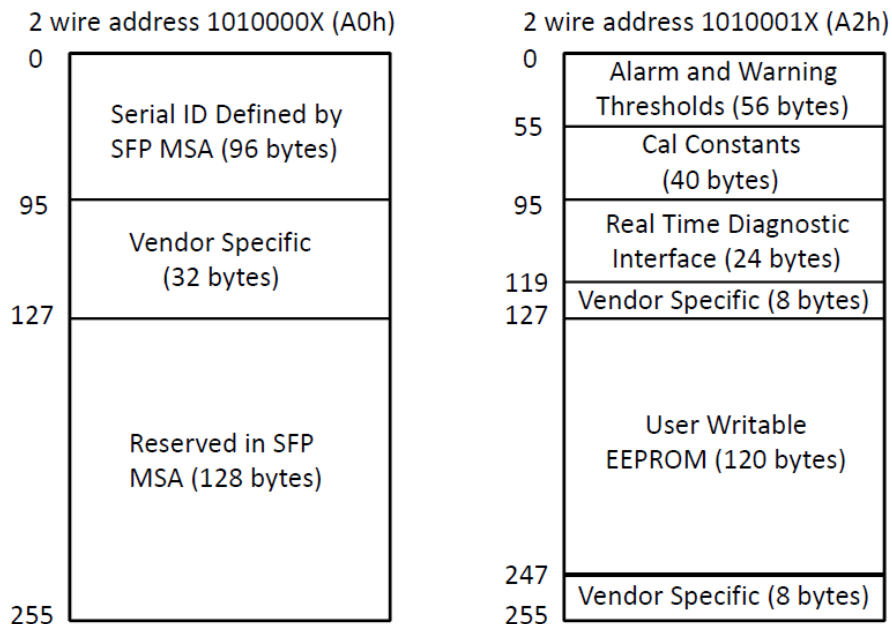
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Recommended Interface Circuit



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7. Digital Diagnostic Memory Map



8. Modification History

Rev.	Comments	Date	Originator	Approval
01	Preliminary Draft	2025.04.17	Albert Lin	Mike Sun

JPC Connectivity